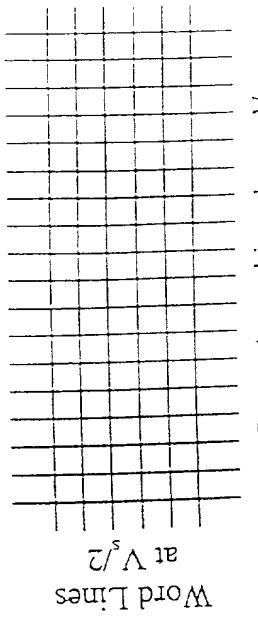


FIG.2

3 Level Passive Matrix Switching Protocol

Maximum depolarizing voltage $V_s/2$

- t_0 : word line latched, active pulldown to 0
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to V_s - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to V_s clamp
- t_8 : read/write cycle complete



Sense Amps biased near V_s

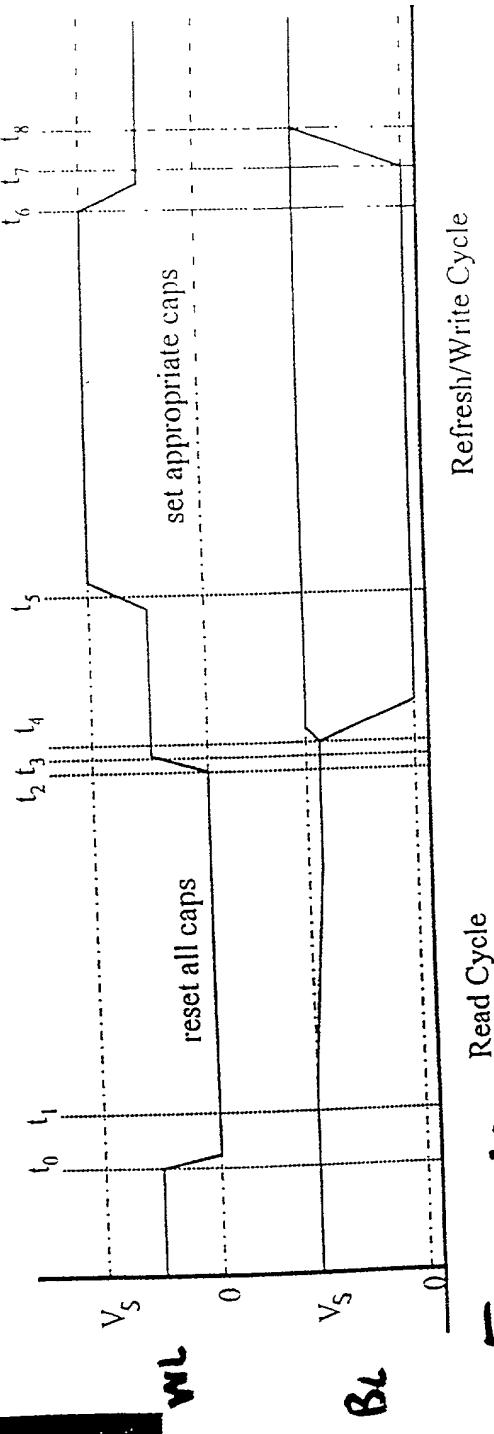
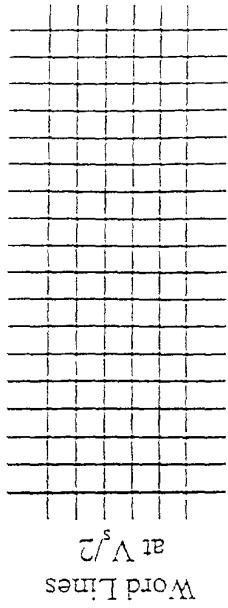


Fig. 4

Refresh/Write Cycle
Read Cycle

3 Level Passive Matrix Switching Protocol

- t_0 : word line latched, active pullup ρ to V_s Maximum depolarizing voltage $V_s/2$
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to 0 - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to 0 clamp
- t_8 : read/write cycle complete



Sense Amps biased near V_s

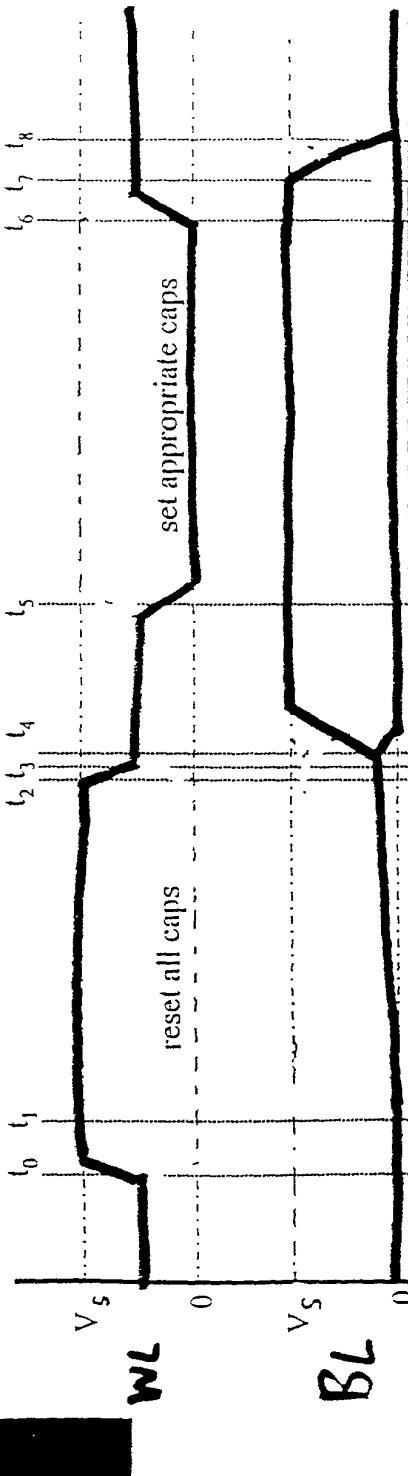


Fig. 5

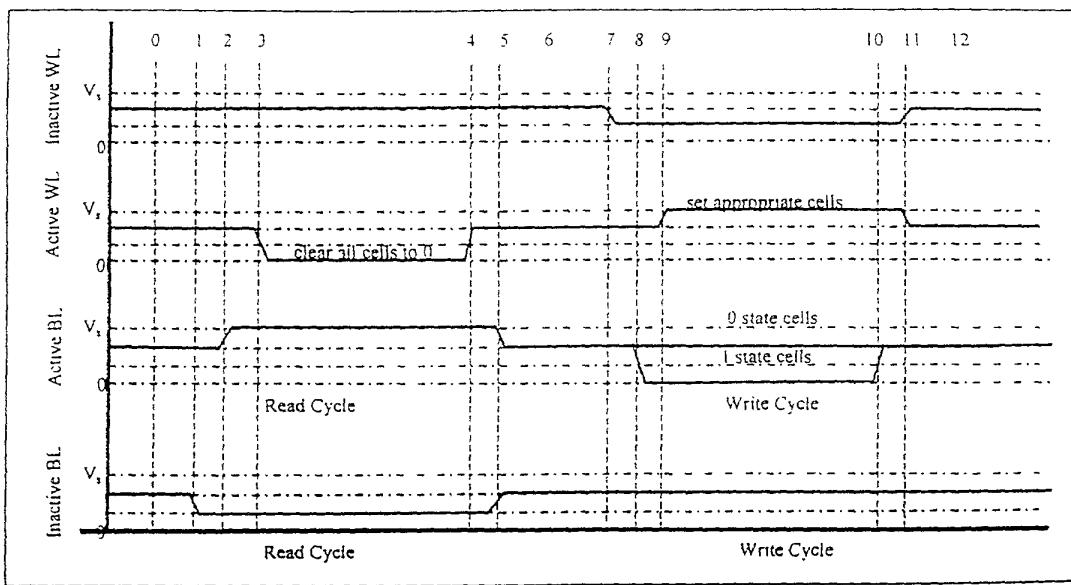
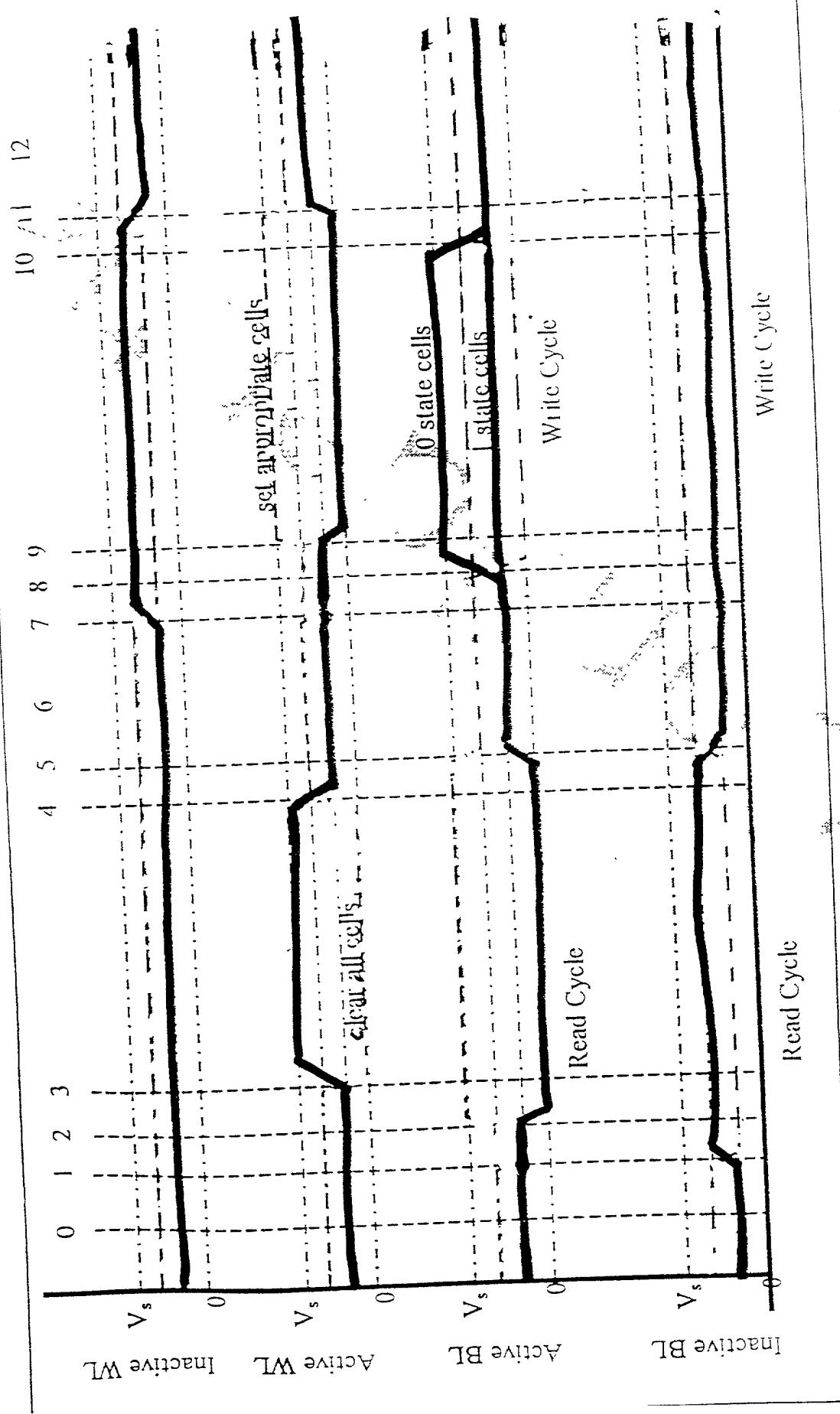


FIG. 6.



F16.7

Five Level Timing Diagram

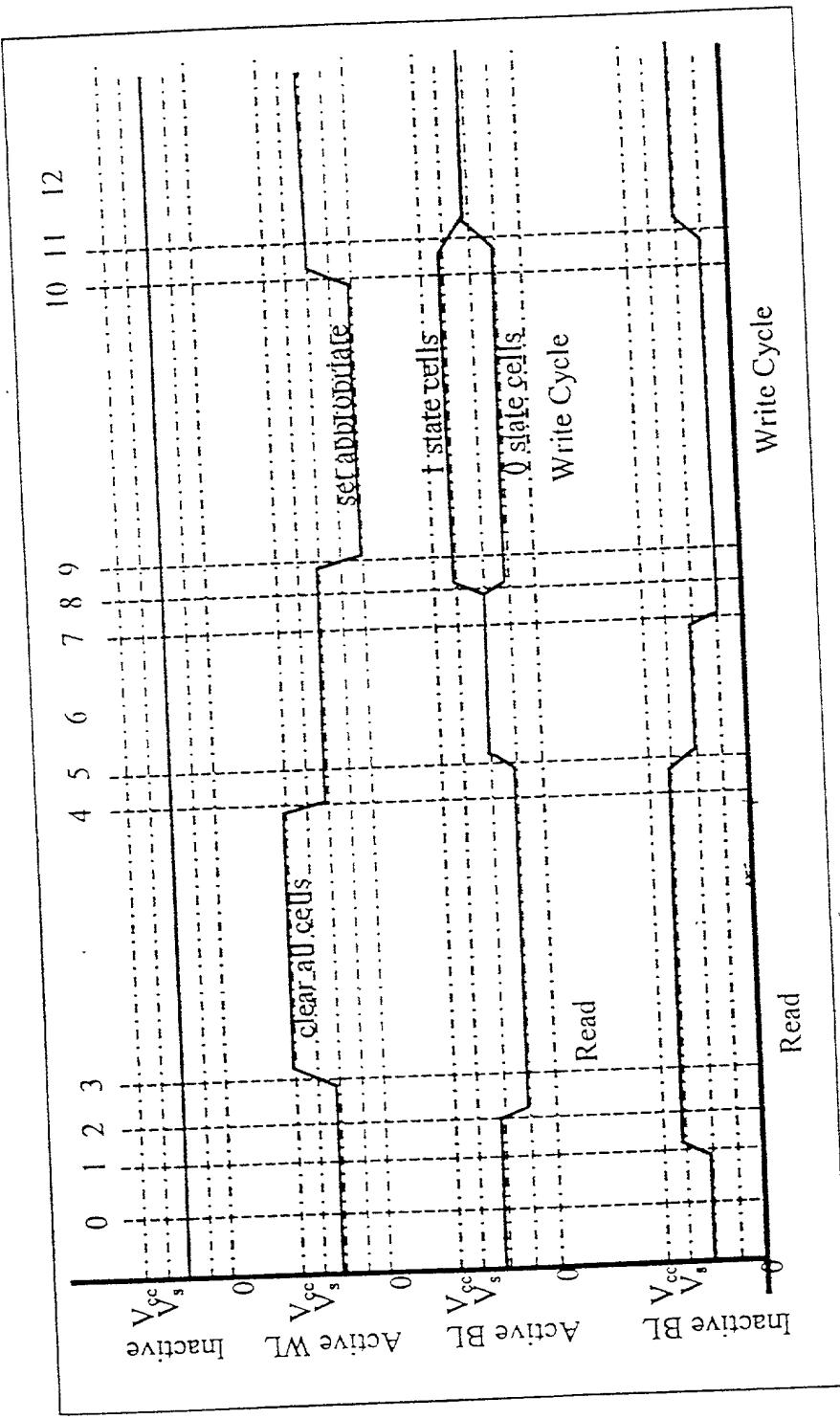
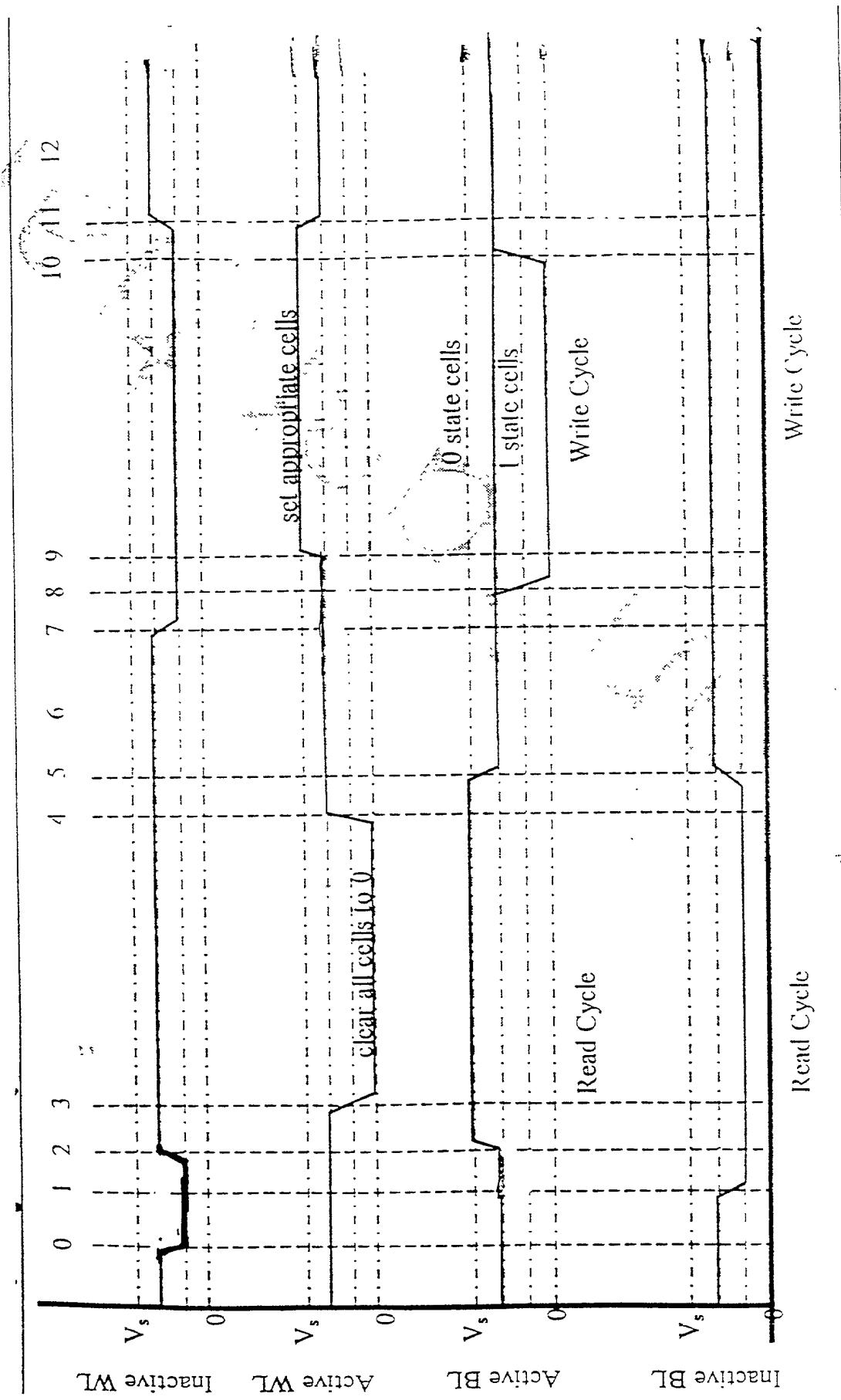
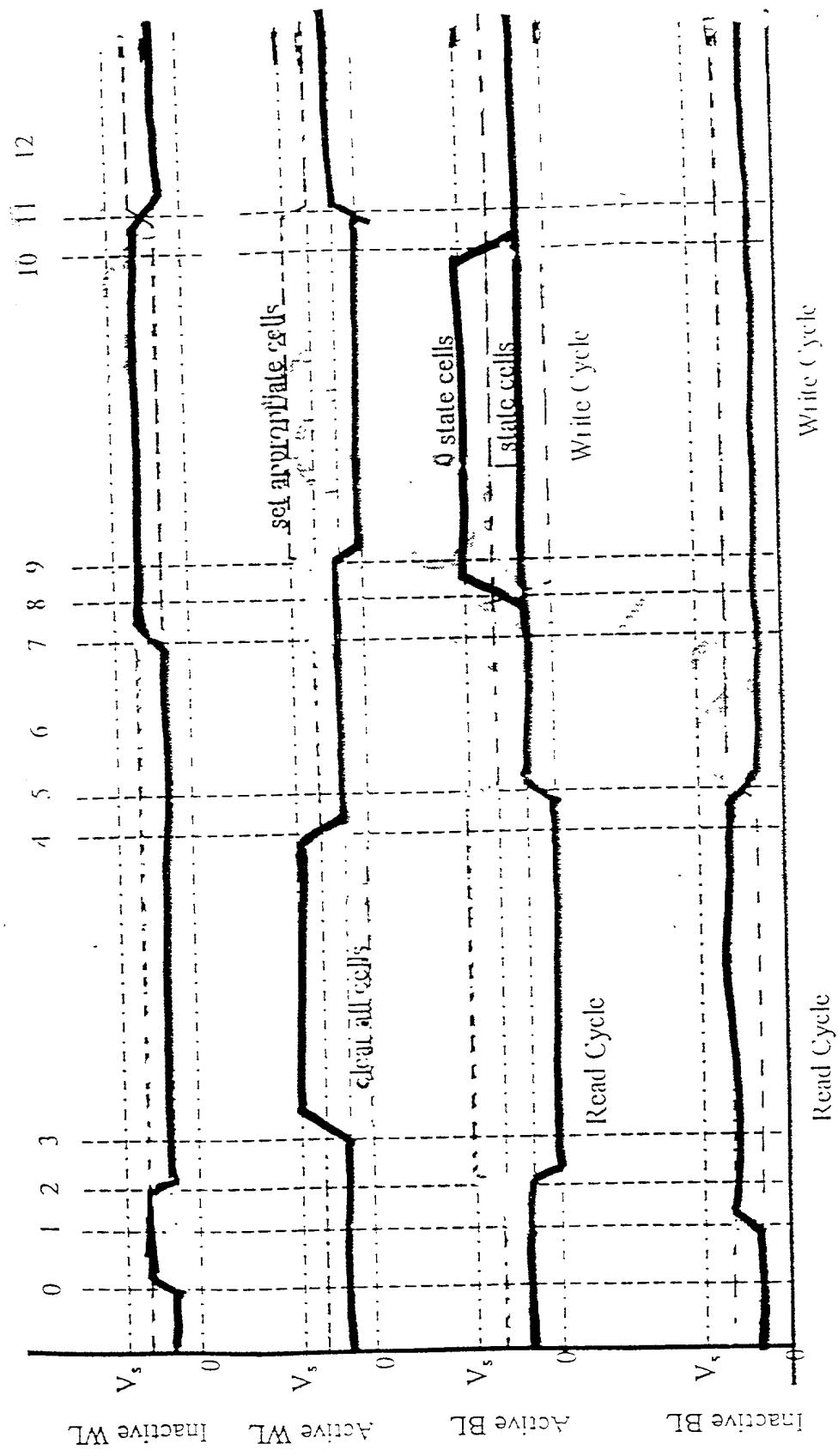


FIG. 9

Fig. 10





F16. 11

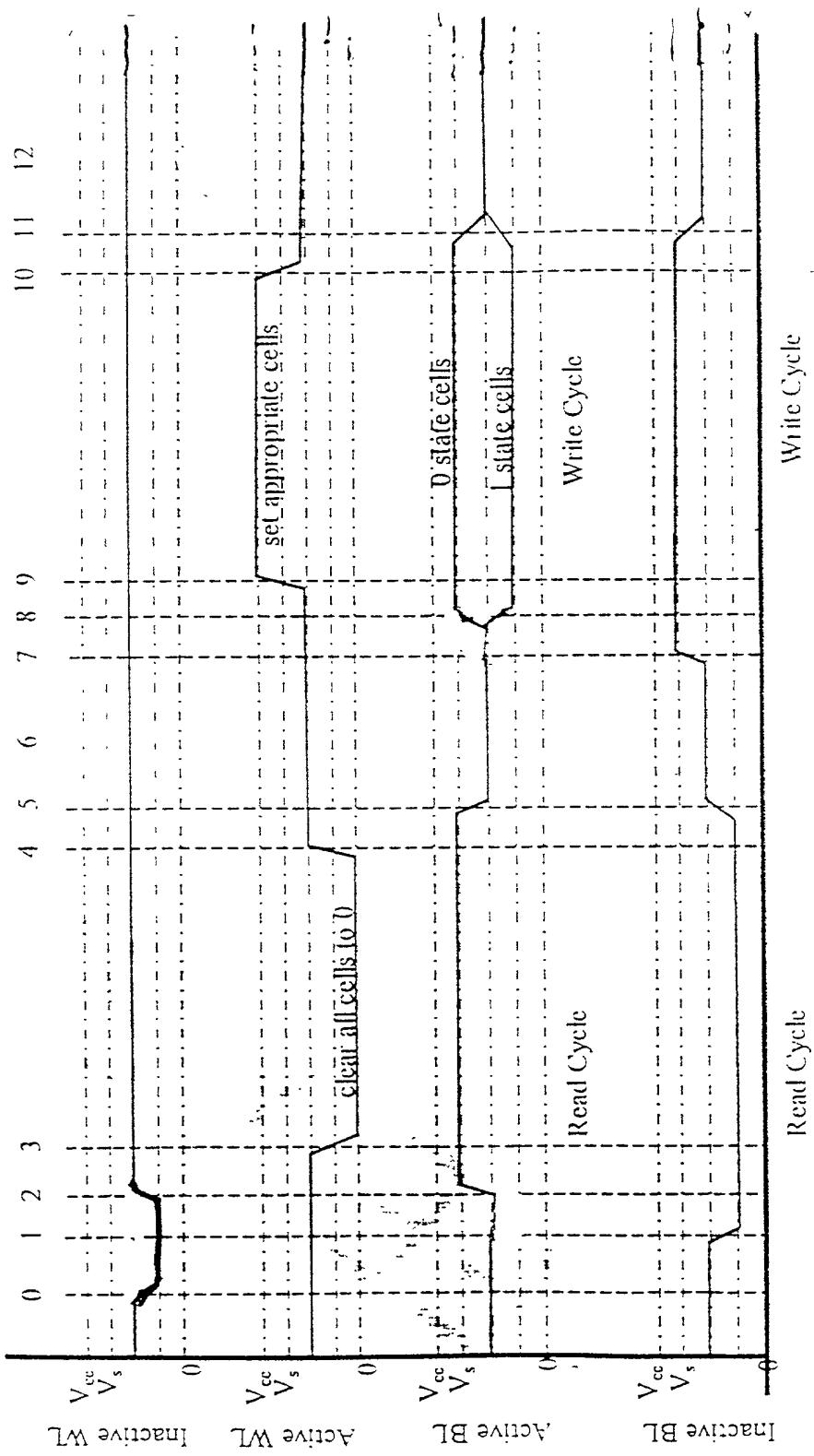


Fig.12.

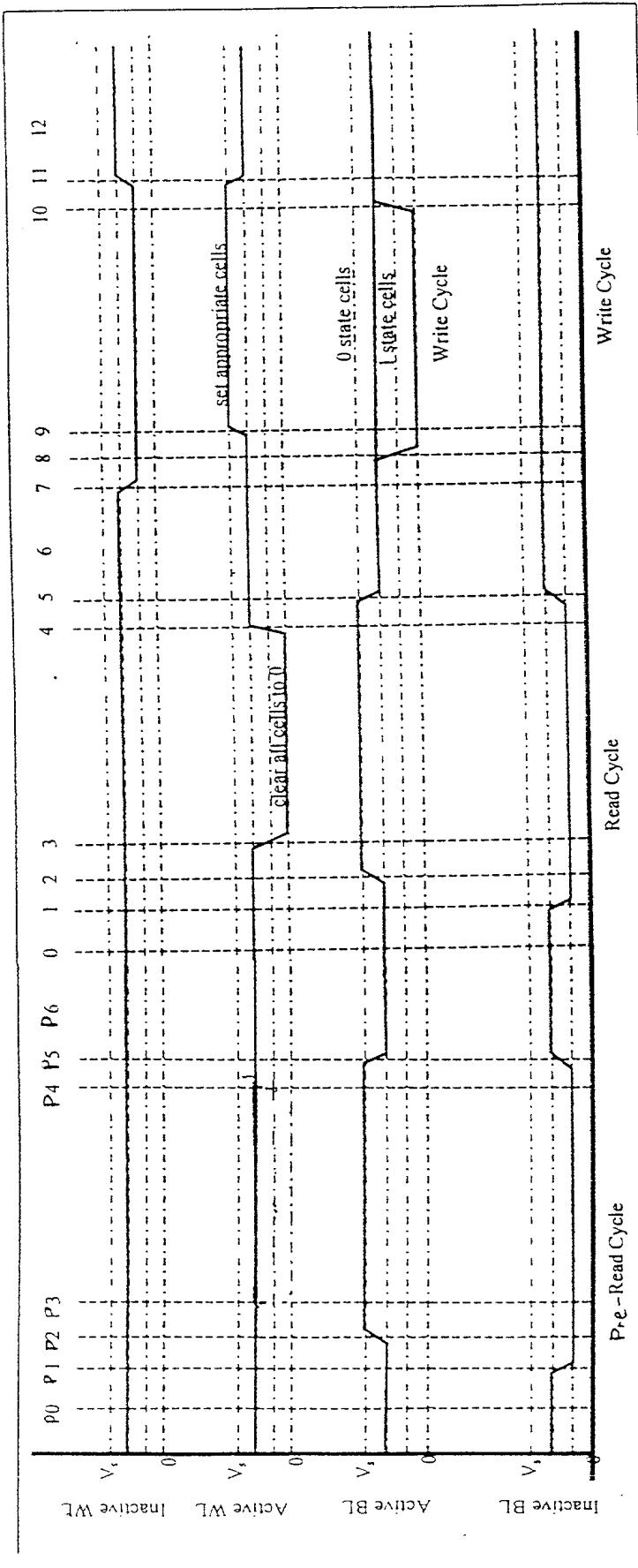


Fig. 14
EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ
REFERENCE CYCLE.

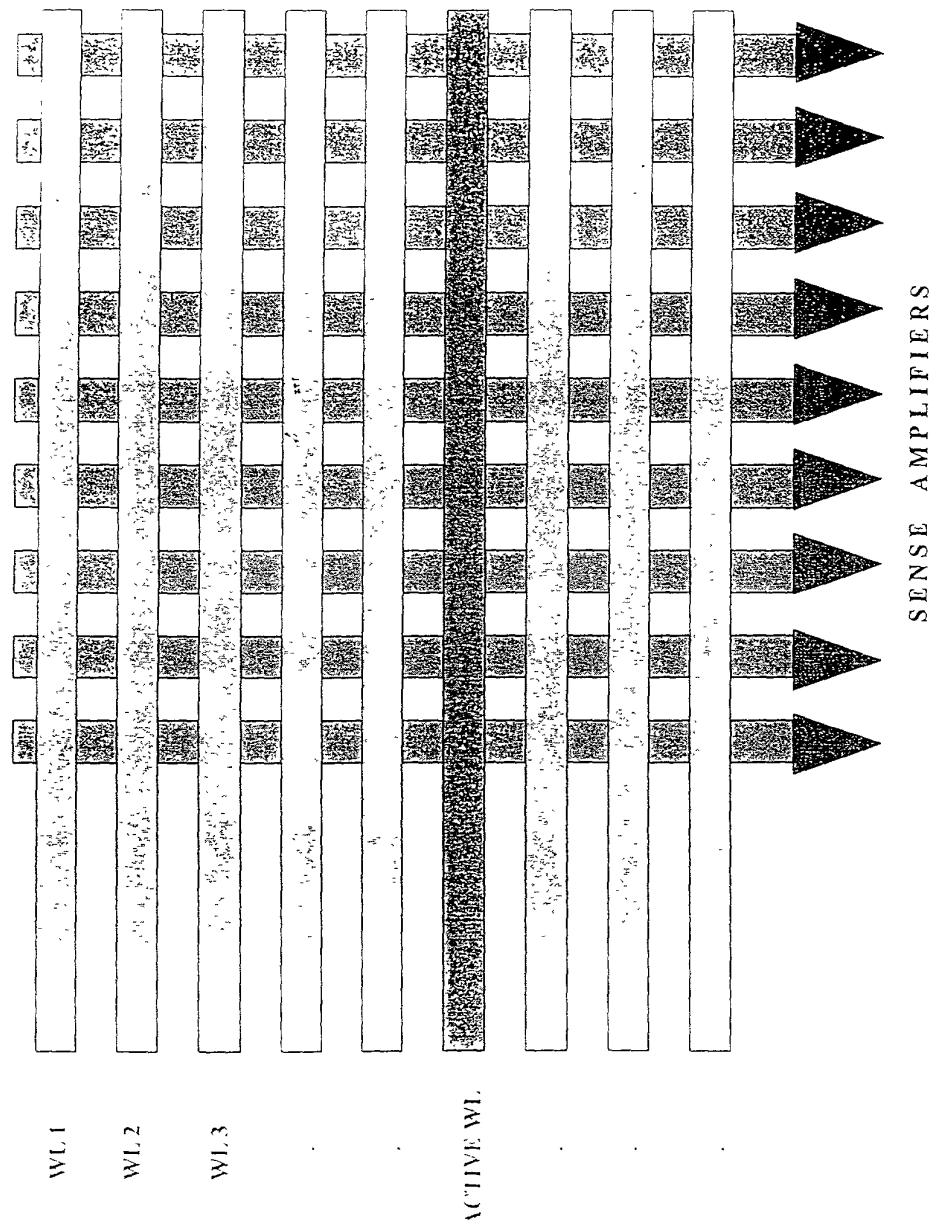


FIG.15